Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) An apparatus comprising:

an integrated circuit (IC) configured for attachment to ~~mounted on~~ a chip carrier, the IC having one or more differential pair circuits coupled thereto, the chip carrier (i) having a signal escaping portion and a remaining portion and (ii) being configured for mounting on a printed circuit board; and

differential signal lines coupled to the differential pair circuits, the differential signal lines (i) extending through the chip carrier and (ii) having first and second segments;

wherein the first segment extends through the escaping portion and the second segment extends through the remaining portion; and

wherein the first and second segments have respective first and second widths.

2. (Original) The apparatus of claim 1, wherein the escaping portion is configured for escaping transmitted signals from the IC.

3. (Original) The apparatus of claim 1, wherein the first and second widths provide substantially uniform impedance characteristics across the signal lines.

4. (Original) The apparatus of claim 3, wherein the impedance is within a range of about 90 to 110 ohms.

5. (Original) The apparatus of claim 1, wherein the second width is larger than the first width.

6. (Original) The apparatus of claim 1, wherein the differential signal lines include respective inverting and non-inverting paths; and

wherein the paths along the escaping portion are separated by a first spacing and the paths along the remaining portion are separated by at least a second spacing.

7. (Original) The apparatus of claim 6, wherein the second spacing is larger that the first spacing.

8. (Original) The apparatus of claim 6, wherein the first and second spacings cooperate to reduce cross-talk between the inverting and non-inverting paths.

9. (Original) The apparatus of claim 6, wherein the first and second widths and the first and second spacings are determined based upon modeling and simulations.

10. (Original) The apparatus of claim 1, wherein the signal lines are configured to transmit high data rate signals.

11. (Original) The apparatus of claim 10, wherein a data rate of the high data rate signals is greater than or equal to about 5 gigabits per second.

12. (Original) The apparatus of claim 6, wherein the inverting and non-inverting paths are adjacent to one another.

13. (Currently Amended) A chip carrier ~~An integrated circuit (IC) (i) having a differential circuit coupled thereto, and (ii)~~ configured for (i) mounting on a printed circuit board, and (ii) attachment to an integrated circuit (IC), the IC having a differential circuit coupled thereto, ~~mounted on a chip carrier~~, the chip carrier ~~differential circuit~~ including a signal escaping portion and a remaining portion, ~~the IC~~ comprising:

differential signal lines extending through the chip carrier and including first and second segments;

wherein the first segment extends through the signal escaping portion and the second segment extends through the remaining portion;

wherein the first and second segments have respective first and second widths; and

wherein the first and second widths provide substantially uniform impedance characteristics across the signal lines.

14. (Currently Amended) The chip carrier ~~IC~~ of claim 13, wherein the first and second widths provide substantially uniform impedance characteristics across the signal lines.

15. (Currently Amended) The chip carrier ~~IC~~ of claim 13, wherein the second width is larger than the first width.

16. (Currently Amended) The chip carrier ~~IC~~ of claim 13, wherein the differential signal lines include respective inverting and non-inverting paths; and

wherein the paths along the escaping portion are separated by a first spacing and the paths along the remaining portion are separated by at least a second spacing.

17. (Currently Amended) The chip carrier ~~IC~~ of claim 16, wherein the second spacing is larger that the first spacing.

18. (Currently Amended) The chip carrier ~~IC~~ of claim 17, wherein the first and second spacings cooperate to reduce cross-talk between the inverting and non-inverting paths.

19. (Currently Amended) The chip carrier ~~IC~~ of claim 18, wherein the first and second widths and the first and second spacings are determined based upon modeling and simulations.

20. (Currently Amended) The chip carrier ~~IC~~ of claim 13, wherein the signal lines are configured to transmit signals having a data-rate greater than about 5 gigabits per second.